### **Always Two Sides To A Story**

#### Siddappa N.Byrareddy

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between forever and always is that always can exist as a "module item", which is the name that the Verilog spec gives to constructs that may be written directly within a module, not contained within some other construct. initial is also a module item. always blocks are repeated, whereas initial blocks are run once at the start of ... Verilog Always block using (\*) symbol - Stack Overflow The always @(\*) syntax was added to the IEEE Verilog Std in 2001. All modern Verilog tools (simulators, synthesis, etc.) support this syntax. Here is a quote from the LRM (1800-2009): An incomplete event\_expression list of an event control is a common source of bugs in register transfer level (RTL) simulations. The implicit event\_expression, @\*, is a ...

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